4/29/06

Refine Search

Search Results -

Terms	Documents
L36 and L26	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L37

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L37	L36 and L26	0	L37
L36	L35 and (contin$6 near stream)	14	L36
L35	L3 and contin$6	542	L35
L34	L3 and contin$	6	L34
L33	L32 and L3	0	L33
L32	711/171.ccls.	533	L32
L31	L30 and L1	0	L31
L30	L27 and (calculat$3 near correlation)	1	L30
L29	L28 and (calculat$3 near correlation)	0	L29
L28	L27 and (threshold near value)	32	L28
L27	L26 and (value near (larger or least))	48	L27
L26	determin$3 same match$3 same coefficient same threshold	412	L26
L25	L24 not L19	0	L25
L24	L23 and L7	1	L24

L23	(L20 or L21 or L22) and L4	25	L23
L22	707/200-206.ccls.	7005	L22
L21	707/100-104.1.ccls.	13659	L21
L20	707/1-10.ccls.	20562	L20
L19	L18 and threshold	1	L19
L18	(L13 or L14 or L15 or L16 or L17) and L4	2	L18
L17	711/145.ccls.	798	L17
L16	711/112.ccls.	1686	L16
L15	711/111.ccls.	843	L15
L14	711/103.ccls.	1636	L14
L13	L12 and l7	1	L13
L12	L11 and L3	25	L12
L11	711/$.ccls.	29314	L11
L10	L9 not L5	3	L10
L9	L7 and L8	4	L9
L8	retriev$3 same ("data signal") same (match$3 or compar$5)	431	L8
L7	"mass storage medium"	1863	L7
L6	L5 and threshold	1	L6
L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L32 and L3	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L33

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L33	L32 and L3	0	L33
L32	711/171.ccls.	533	L32
L31	L30 and L1	0	L31
L30	L27 and (calculat$3 near correlation)	1	L30
L29	L28 and (calculat$3 near correlation)	0	L29
L28	L27 and (threshold near value)	32	L28
L27	L26 and (value near (larger or least))	48	L27
L26	determin$3 same match$3 same coefficient same threshold	412	L26
L25	L24 not L19	0	L25
L24	L23 and L7	1	L24
L23	(L20 or L21 or L22) and L4	25	L23
L22	707/200-206.ccls.	7005	L22
L21	707/100-104.1.ccls.	13659	L21
L20	707/1-10.ccls.	20562	L20

L19	L18 and threshold	1	L19
L18	(L13 or L14 or L15 or L16 or L17) and L4	2	L18
L17	711/145.ccls.	798	L17
L16	711/112.ccls.	1686	L16
L15	711/111.ccls.	843	L15
L14	711/103.ccls.	1636	L14
L13	L12 and l7	1	L13
L12	L11 and L3	25	L12
L11	711/$.ccls.	29314	L11
L10	L9 not L5	3	L10
L9	L7 and L8	4	L9
L8	retriev$3 same ("data signal") same (match$3 or compar$5)	431	L8
L7	"mass storage medium"	1863	L7
L6	L5 and threshold	1	L6
L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

4/29/06 mw

Refine Search

Search Results -

Terms	Documents
L30 and L1	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L31

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L31	L30 and L1	0	L31
L30	L27 and (calculat$3 near correlation)	1	L30
L29	L28 and (calculat$3 near correlation)	0	L29
L28	L27 and (threshold near value)	32	L28
L27	L26 and (value near (larger or least))	48	L27
L26	determin$3 same match$3 same coefficient same threshold	412	L26
L25	L24 not L19	0	L25
L24	L23 and L7	1	L24
L23	(L20 or L21 or L22) and L4	25	L23
L22	707/200-206.ccls.	7005	L22
L21	707/100-104.1.ccls.	13659	L21
L20	707/1-10.ccls.	20562	L20
L19	L18 and threshold	1	L19
L18	(L13 or L14 or L15 or L16 or L17) and L4	2	L18

L17	711/145.ccls.	798	L17
L16	711/112.ccls.	1686	L16
L15	711/111.ccls.	843	L15
L14	711/103.ccls.	1636	L14
L13	L12 and l7	1	L13
L12	L11 and L3	25	L12
L11	711/$.ccls.	29314	L11
L10	L9 not L5	3	L10
L9	L7 and L8	4	L9
L8	retriev$3 same ("data signal") same (match$3 or compar$5)	431	L8
L7	"mass storage medium"	1863	L7
L6	L5 and threshold	1	L6
L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L28 and (calculat$3 near correlation)	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L29

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L29	L28 and (calculat$3 near correlation)	0	L29
L28	L27 and (threshold near value)	32	L28
L27	L26 and (value near (larger or least))	48	L27
L26	determin$3 same match$3 same coefficient same threshold	412	L26
L25	L24 not L19	0	L25
L24	L23 and L7	1	L24
L23	(L20 or L21 or L22) and L4	25	L23
L22	707/200-206.ccls.	7005	L22
L21	707/100-104.1.ccls.	13659	L21
L20	707/1-10.ccls.	20562	L20
L19	L18 and threshold	1	L19
L18	(L13 or L14 or L15 or L16 or L17) and L4	2	L18
L17	711/145.ccls.	798	L17
L16	711/112.ccls.	1686	L16

L15	711/111.ccls.	843	L15
L14	711/103.ccls.	1636	L14
L13	L12 and l7	1	L13
L12	L11 and L3	25	L12
L11	711/$.ccls.	29314	L11
L10	L9 not L5	3	L10
L9	L7 and L8	4	L9
L8	retriev$3 same ("data signal") same (match$3 or compar$5)	431	L8
L7	"mass storage medium"	1863	L7
L6	L5 and threshold	1	L6
L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

4/29/06 jmc

Refine Search

Search Results -

Terms	Documents
L5 and threshold	1

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5 and threshold	1	L6
L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6711558 B1

Using default format because multiple data bases are involved.

L6: Entry 1 of 1 File: USPT Mar 23, 2004

US-PAT-NO: 6711558
DOCUMENT-IDENTIFIER: US 6711558 B1

TITLE: Associative database scanning and information retrieval

DATE-ISSUED: March 23, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Indeck; Ronald S.	St. Louis	MO		
Cytron; Ron Kaplan	St. Louis	MO		
Franklin; Mark Allen	St. Louis	MO		

US-CL-CURRENT: 707/1; 707/3, 709/225, 711/112

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L5 and threshold	1

Display Format: - Change Format

Previous Page Next Page Go to Doc#

4/29/06

Refine Search

Search Results -

Terms	Documents
L18 and threshold	1

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L19

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L19	L18 and threshold	1	L19
L18	(L13 or L14 or L15 or L16 or L17) and L4	2	L18
L17	711/145.ccls.	798	L17
L16	711/112.ccls.	1686	L16
L15	711/111.ccls.	843	L15
L14	711/103.ccls.	1636	L14
L13	L12 and l7	1	L13
L12	L11 and L3	25	L12
L11	711/$.ccls.	29314	L11
L10	L9 not L5	3	L10
L9	L7 and L8	4	L9
L8	retriev$3 same ("data signal") same (match$3 or compar$5)	431	L8
L7	"mass storage medium"	1863	L7
L6	L5 and threshold	1	L6

L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6711558 B1

Using default format because multiple data bases are involved.

L19: Entry 1 of 1 File: USPT Mar 23, 2004

US-PAT-NO: 6711558
DOCUMENT-IDENTIFIER: US 6711558 B1

TITLE: Associative database scanning and information retrieval

DATE-ISSUED: March 23, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Indeck; Ronald S.	St. Louis	MO		
Cytron; Ron Kaplan	St. Louis	MO		
Franklin; Mark Allen	St. Louis	MO		

US-CL-CURRENT: 707/1; 707/3, 709/225, 711/112

Full | Title | Citation | Front | Review | Classification | Date | Reference | References | Attachments | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L18 and threshold	1

Display Format: - Change Format

Previous Page Next Page Go to Doc#

4/29/06

Refine Search

Search Results -

Terms	Documents
L24 not L19	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L25

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L25	L24 not L19	0	L25
L24	L23 and L7	1	L24
L23	(L20 or L21 or L22) and L4	25	L23
L22	707/200-206.ccls.	7005	L22
L21	707/100-104.1.ccls.	13659	L21
L20	707/1-10.ccls.	20562	L20
L19	L18 and threshold	1	L19
L18	(L13 or L14 or L15 or L16 or L17) and L4	2	L18
L17	711/145.ccls.	798	L17
L16	711/112.ccls.	1686	L16
L15	711/111.ccls.	843	L15
L14	711/103.ccls.	1636	L14
L13	L12 and l7	1	L13
L12	L11 and L3	25	L12

L11	711/$.ccls.	29314	L11
L10	L9 not L5	3	L10
L9	L7 and L8	4	L9
L8	retriev$3 same ("data signal") same (match$3 or compar$5)	431	L8
L7	"mass storage medium"	1863	L7
L6	L5 and threshold	1	L6
L5	L4 and (correlat$4 same key)	3	L5
L4	L3 and retriev$3	322	L4
L3	L1 and L2	644	L3
L2	pattern near (comparison or match$)	31590	L2
L1	("Field Programmable Gate Arrays") or FPGA	30488	L1

END OF SEARCH HISTORY

4/29/06

Refine Search

Search Results -

Terms	Documents
L10 and L2	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L11

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L11	L10 and L2	0	L11
L10	L9 and L1	19	L10
L9	709/214.ccls.	359	L9
L8	L7 and (pattern same match$3)	1	L8
L7	L6 and L1	8	L7
L6	L5 and L3	113	L6
L5	709/$.ccls.	44194	L5
L4	L1 and L2 and L3	2	L4
L3	"mass storage medium"	1863	L3
L2	pattern near (compar$6 or match$3)	45889	L2
L1	"Field Programmable gate Array" or FPGA	30488	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L18 and coefficient	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L19

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, April 29, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L19	L18 and coefficient	0	L19
L18	L17 and (threshold near value)	1	L18
L17	L16 and (pattern same compar$6)	5	L17
L16	L15 and retriev$3	8	L16
L15	L12 and (pattern same match$3)	12	L15
L14	L12 and l1 and L3	0	L14
L13	L12 and l1 and L2	0	L13
L12	711/1.ccls.	524	L12
L11	L10 and L2	0	L11
L10	L9 and L1	19	L10
L9	709/214.ccls.	359	L9
L8	L7 and (pattern same match$3)	1	L8
L7	L6 and L1	8	L7
L6	L5 and L3	113	L6

L5	709/$.ccls.	44194	L5
L4	L1 and L2 and L3	2	L4
L3	"mass storage medium"	1863	L3
L2	pattern near (compar$6 or match$3)	45889	L2
L1	"Field Programmable gate Array" or FPGA	30488	L1

END OF SEARCH HISTORY

Terms used **mass storage medium Field Programmable Gate Arrays retrieval device pattern comparison continuous correlation coefficient value least predetermined threshold value**

Found **1** of **175,083**

Sort results by: relevance
Display results: expanded form
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Results 1 - 1 of 1

Relevance scale

1 Content inspection: High-throughput linked-pattern matching for intrusion detection systems

Zachary K. Baker, Viktor K. Prasanna
October 2005 **Proceedings of the 2005 symposium on Architecture for networking and communications systems ANCS '05**
Publisher: ACM Press
Full text available: pdf(300.66 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a hardware architecture for highly efficient intrusion detection systems. In addition, a software tool for automatically generating the hardware is presented.Intrusion detection for network security is a compute-intensive application demanding high system performance. By moving both the string matching and the linking of multi-part rules to hardware, our architecture leaves the host system free for higher-level analysis. The tool automates the creation of efficient Field Prog ...

Keywords: network intrusion detection, string matching

Results 1 - 1 of 1

Terms used **mass storage medium Field Programmable Gate Arrays retrieval device pattern comparison correlation coefficient value large threshold value**

Found **5** of **175,083**

Sort results by: relevance

Display results: expanded form

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Results 1 - 5 of 5

Relevance scale

1 Combinational logic synthesis for LUT based field programmable gate arrays

Jason Cong, Yuzheng Ding

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Publisher: ACM Press

Full text available: pdf(628.91 KB) Additional Information: full citation, abstract, references, citings, index terms, review

The increasing popularity of the field programmable gate-array (FPGA) technology has generated a great deal of interest in the algorithmic study and tool development for FPGA-specific design automation problems. The most widely used FPGAs are LUT based FPGAs, in which the basic logic element is a K-input one-output lookup-table (LUT) that can implement any Boolean function of up to K variables. This unique feature of the LUT has brought new challenges to lo ...

Keywords: FPGA, area minimization, computer-aided design of VLSI, decomposition, delay minimization, delay modeling, logic optimization, power minimization, programmable logic, routing, simplification, synthesis, system design, technology mapping

2 Sequencing run-time reconfigured hardware with software

Michael J. Wirthlin, Brad L. Hutchings

February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(220.45 KB) Additional Information: full citation, references, citings, index terms

3 Performance-driven mapping for CPLD architectures

Deming Chen, Jason Cong, Milos D. Ercegovac, Zhijun Huang

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(265.58 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a performance-driven mapping algorithm, PLAmap, for CPLD architectures which consist of a large number of PLA-style logic cells. The primary goal of our mapping algorithm is to minimize the depth of the mapped circuit. Meanwhile, we have successfully reduced the area of the mapped circuits by applying several heuristic techniques, including threshold control of PLA fanouts and product terms, slack-time relaxation, and PLA-packing. We compare our PLAmap with a recent ...

Keywords: CPLD, FPGA, PLA-style logic cells, delay optimization, technology mapping

4 Novel devices and approaches to programmable devices: A magnetoelectronic macrocell employing reconfigurable threshold logic

Steve P. Ferrera, Nicholas P. Carter

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(288.34 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we introduce a reconfigurable fabric based around a new class of circuit element: the hybrid Hall effect (HHE) magnetoelectronic device. Because they incorporate a ferromagnetic element, HHE devices are inherently non-volatile, retaining their state without a power supply. In addition, HHE devices are extremely well-suited to implementing threshold logic circuits, which allows many complex logic functions to be implemented in fewer gates than are required in systems based on AND-O ...

Keywords: PLA/CPLD, lookup table, magnetoelectronic circuits, non-volatility, threshold logic, wired-and logic

5 Reconfigurable systems: Efficient LUT-based FPGA technology mapping for power minimization

Hao Li, Wai-Kei Mak, Srinivas Katkoori

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

Publisher: ACM Press

Full text available: pdf(208.62 KB) Additional Information: full citation, abstract, references

We study the technology mapping problem for LUT-based FPGAs targeting at power minimization. The problem has been proved to be NP-hard previously. Hence, we present an efficient heuristic to compute low-power mapping solutions. The major distinction of our work from previous ones is that while generating a LUT, we look ahead at the impact of the mapping selection of this LUT on the power consumption of the remaining network. We choose the mapping that results in the least estimated overall power ...

Results 1 - 5 of 5

Terms used **mass storage medium Field Programmable Gate Arrays retrieval device pattern comparison continuous correlation coefficient value least threshold value**

Found **21** of **175,083**

Sort results by relevance

Display results expanded form

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Results 1 - 20 of 21 Result page: **1** 2

Relevance scale

1 System-on-chip communication and reconfigurable systems: A continuous-time hierarchical field programmable analogue array for rapid prototyping and hierarchical approach to analogue systems design

David Varghese, J. N. Ross

September 2005 **Proceedings of the 18th annual symposium on Integrated circuits and system design SBCCI '05**

Publisher: ACM Press

Full text available: pdf(653.82 KB) Additional Information: full citation, abstract, references, index terms

This paper presents our continuous-time Hierarchical Field Programmable Analogue Array (HFPAA) designed as a result of our research efforts to enable rapid prototyping for analogue system design. Here, we present our continuous-time configurable analogue block (CAB) used for our HFPAA, with increased flexibility in facilitating a hierarchical approach to analogue design and also in configuring target applications. This is achieved by minimising the dependence of our CAB on external passive compo ...

Keywords: FPAA, HFPAA, differential difference amplifier, hierarchical architecture, interconnectivity analysis, non-permuting grouped combinations listing algorithm, rents rule, second generation current-conveyor

2 Performance-driven mapping for CPLD architectures

Deming Chen, Jason Cong, Milos D. Ercegovac, Zhijun Huang

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(265.58 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a performance-driven mapping algorithm, PLAmap, for CPLD architectures which consist of a large number of PLA-style logic cells. The primary goal of our mapping algorithm is to minimize the depth of the mapped circuit. Meanwhile, we have successfully reduced the area of the mapped circuits by applying several heuristic techniques, including threshold control of PLA fanouts and product terms, slack-time relaxation, and PLA-packing. We compare our PLAmap with a recent ...

Keywords: CPLD, FPGA, PLA-style logic cells, delay optimization, technology mapping

3 System architectures for computer music

John W. Gordon
June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2
Publisher: ACM Press

Full text available: pdf(4.61 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

4 Error detection for adaptive computing architectures in spacecraft applications

David Brodrick, Anwar Dawood, Neil Bergmann, Melanie Wark
January 2001 **Australian Computer Science Communications , Proceedings of the 6th Australasian conference on Computer systems architecture ACSAC '01**, Volume 23 Issue 4
Publisher: IEEE Computer Society , IEEE Computer Society Press

Full text available: pdf(803.02 KB) Publisher Site Additional Information: full citation, abstract, references

The Australian FedSat satellite will incorporate a payload to validate the use of adaptive computing architectures in spacecraft applications. The technology has many exciting benefits for deployment in spacecraft, but the space environment also represents unique challenges which must be addressed. An important consideration is that modern SRAM Field Programmable Gate Arrays (FPGAs), such as the Xilinx 4000 device used on FedSat, are vulnerable to a range of radiation induced errors. A system is ...

5 Special section on data mining for intrusion detection and threat analysis: Mining system audit data: opportunities and challenges

Wenke Lee, Wei Fan
December 2001 **ACM SIGMOD Record**, Volume 30 Issue 4
Publisher: ACM Press

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

Intrusion detection is an essential component of computer security mechanisms. It requires accurate and efficient analysis of a large amount of system and network audit data. It can thus be an application area of data mining. There are several characteristics of audit data: abundant raw data, rich system and network semantics, and ever "streaming". Accordingly, when developing data mining approaches, we need to focus on: feature extraction and construction, customization of (general) algorithms ...

6 Boolean satisfiability in electronic design automation

João P. Marques-Silva, Karem A. Sakallah
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(55.32 KB) Additional Information: full citation, abstract, references, citings, index terms

Boolean Satisfiability (SAT) is often used as the underlying model for a significant and increasing number of applications in Electronic Design Automation (EDA) as well as in many other fields of Computer Science and Engineering. In recent years, new and

efficient algorithms for SAT have been developed, allowing much larger problem instances to be solved. SAT "packages" are currently expected to have an impact on EDA applications similar to that of BDD packages since the ...

7 Logic synthesis and mapping: Using logic duplication to improve performance in FPGAs

Karl Schabas, Stephen D. Brown

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(238.48 KB) Additional Information: full citation, abstract, references, citings, index terms

The purpose of this paper is to introduce a modified packing and placement algorithm for FPGAs that utilizes logic duplication to improve performance. The modified packing algorithm was designed to leave unused basic logic elements (BLEs) in timing critical clusters, to allow potential targets for logic duplication. The modified placement algorithm consists of a new stage after placement in which logic duplication is performed to shorten the length of the critical path. In this paper, we show th ...

Keywords: FPGA, logic duplication

8 Content inspection: High-throughput linked-pattern matching for intrusion detection systems

Zachary K. Baker, Viktor K. Prasanna

October 2005 **Proceedings of the 2005 symposium on Architecture for networking and communications systems ANCS '05**

Publisher: ACM Press

Full text available: pdf(300.66 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a hardware architecture for highly efficient intrusion detection systems. In addition, a software tool for automatically generating the hardware is presented.Intrusion detection for network security is a compute-intensive application demanding high system performance. By moving both the string matching and the linking of multi-part rules to hardware, our architecture leaves the host system free for higher-level analysis. The tool automates the creation of efficient Field Prog ...

Keywords: network intrusion detection, string matching

9 Power minimization algorithms for LUT-based FPGA technology mapping

Hao Li, Srinivas Katkoori, Wai-Kei Mak

January 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 1

Publisher: ACM Press

Full text available: pdf(141.02 KB) Additional Information: full citation, abstract, references, index terms

We study the technology mapping problem for LUT-based FPGAs targeting at power minimization. The problem has been proved to be NP-hard previously. Therefore, we present an efficient heuristic algorithm to generate low-power mapping solutions. The key idea is to compute and select low-power *K*-feasible cuts by an efficient incremental network flow computation method. Experimental results show that our algorithm reduces power consumption as well as area over the best algorithms reported in t ...

Keywords: Delay minimization, FPGA, power optimization, technology mapping

10 A new connection admission control for spotbeam handover in LEO satellite networks
Sungrae Cho, Ian F. Akyildiz, Michael D. Bender, Huseyin Uzunalioğlu
July 2002 **Wireless Networks**, Volume 8 Issue 4
Publisher: Kluwer Academic Publishers
Full text available: pdf(313.30 KB) Additional Information: full citation, abstract, references, index terms

Frequent spotbeam handovers in *low earth orbit* (LEO) satellite networks require a technique to decrease the handover blocking probabilities. A large variety of schemes have been proposed to achieve this goal in terrestrial mobile cellular networks. Most of them focus on the notion of prioritized channel allocation algorithms. However, these schemes cannot provide the connection-level *quality of service* (QoS) guarantees. Due to the scarcity of resources in LEO satellite networks, a ...

Keywords: LEO satellite networks, channel allocation, connection admission control, handover management

11 Discovering information flow suing high dimensional conceptual space
Dawei Song, Peter Bruza
September 2001 **Proceedings of the 24th annual international ACM SIGIR conference on Research and development in information retrieval**
Publisher: ACM Press
Full text available: pdf(241.82 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an informational inference mechanism realized via the use of a high dimensional conceptual space. More specifically, we claim to have operationalized important aspects of G„rdenforss recent three-level cognitive model. The connectionist level is primed with the Hyperspace Analogue to Language (HAL) algorithm which produces vector representations for use at the conceptual level. We show how inference at the symbolic level can be implemented by employing Barwise and Seligm ...

Keywords: conceptual space, information flow, informational inference

12 A FPGA-based implementation of a fault-tolerant neural architecture for photon identification
M. Alderighi, E. L. Gummati, V. Piuri, G. R. Sechi
February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(965.46 KB) Additional Information: full citation, references, citings, index terms

13 Document structure and content analysis 2: Schema matching for transforming structured documents
Aida Boukottaya, Christine Vanoirbeek
November 2005 **Proceedings of the 2005 ACM symposium on Document engineering DocEng '05**
Publisher: ACM Press
Full text available: pdf(441.70 KB) Additional Information: full citation, abstract, references, index terms

Structured document content reuse is the problem of restructuring and translating data structured under a source schema into an instance of a target schema. A notion closely tied with structured document reuse is that of structure transformations. Schema

matching is a critical strep in structured document transformations. Manual matching is expensive and error-prone. It is therefore important to develop techniques to automate the matching process and thus the transformation process. In this pape ...

Keywords: document structure transformations, schema matching

14 A delay driven FPGA placement algorithm
Srilata Raman, C. L. Liu, Larry G. Jones
September 1994 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(588.67 KB) Additional Information: full citation, references, citings, index terms

15 Programming combined discrete-continuous simulation models for performance
J. Frederick Klingener
November 1996 **Proceedings of the 28th conference on Winter simulation**
Publisher: ACM Press
Full text available: pdf(683.15 KB) Additional Information: full citation, references, citings

16 Systems: Sensor node selection for execution of continuous probabilistic queries in wireless sensor networks
Kam-Yiu Lam, Reynold Cheng, BiYu Liang, Jo Chau
October 2004 **Proceedings of the ACM 2nd international workshop on Video surveillance & sensor networks**
Publisher: ACM Press
Full text available: pdf(315.34 KB) Additional Information: full citation, abstract, references, index terms

Due to the error-prone properties of sensors, it is important to use multiple low-cost sensors to improve the reliability of query results. However, using multiple sensors to generate the value for a data item can be expensive, especially in wireless environments where continuous queries are executed. Further, we need to distinguish effectively which sensors are not working properly and discard them from being used. In this paper, we propose a probabilistic approach to decide w ...

Keywords: continuous probabilistic query, sensor network

17 Measurement and empirical software engineering: A proposal for using continuous attributes in classification trees
Sandro Morasca
July 2002 **Proceedings of the 14th international conference on Software engineering and knowledge engineering SEKE '02**
Publisher: ACM Press
Full text available: pdf(155.38 KB) Additional Information: full citation, abstract, references, index terms

Classification trees have been successfully used in several application fields. However, continuous attributes cannot be used directly when building classification trees, but they must be first discretized with clustering techniques, which require some degree of subjectivity. We propose an approach to build classification trees that does not require the discretization of the continuous attributes. The approach is an extension of existing methods for building classification trees and is based on ...

Keywords: C4.5, ID3, continuous attributes, decision trees

18 Experimental evaluation of PFS continuous media file system

Wonjun Lee, Difu Su, Duminda Wijesekera, Jaideep Srivastava, Deepak Kenchammana-Hosekote, Mark Foresti

January 1997 **Proceedings of the sixth international conference on Information and knowledge management**

Publisher: ACM Press

Full text available: pdf(1.14 MB) Additional Information: full citation, references, citings, index terms

19 Combined discrete-continuous simulation models in ProModel for Windows

J. Frederick Klingener

December 1995 **Proceedings of the 27th conference on Winter simulation**

Publisher: ACM Press

Full text available: pdf(573.25 KB) Additional Information: full citation, references, citings, index terms

20 Continuous learning: a design methodology for fault-tolerant neural networks

Vincenzo Piuri

June 1990 **Proceedings of the 3rd international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2 IEA/AIE '90**

Publisher: ACM Press

Full text available: pdf(1.36 MB) Additional Information: full citation, abstract, references, index terms

Fault tolerance in artificial neural networks is an important feature, in particular when the application is critical or when maintenance is difficult. This paper presents a general design methodology for designing fault-tolerant architectures, starting from the behavioral description of the nominal network and from the nominal algorithm. The behavioral.level is considered to detect errors due to hardware faults, while system survival is guaranteed by the reactivation of learning mechanisms ...

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